4-UART Chip CH9434

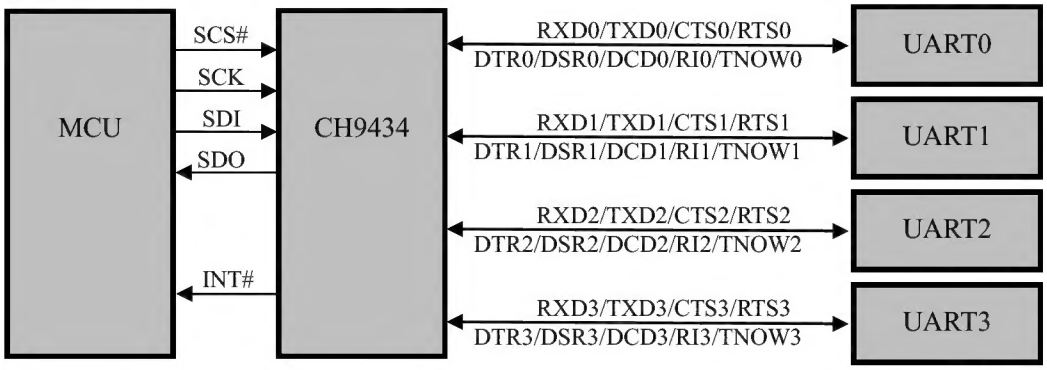
Datasheet

Version: 1A

http://wch.cn

1. Overview

CH9434 is a SPI to 4-UART transfer chip, which provides four full duplex nine-line UARTs, and is used to extend UART for MCU/embedded system. CH9434 includes four UARTs compatible with 16C550 and supports up to 4Mbps baud rate communication. It supports up to 25-channel GPIO and provides half-duplex transceiver automatic switch pin TNOW.



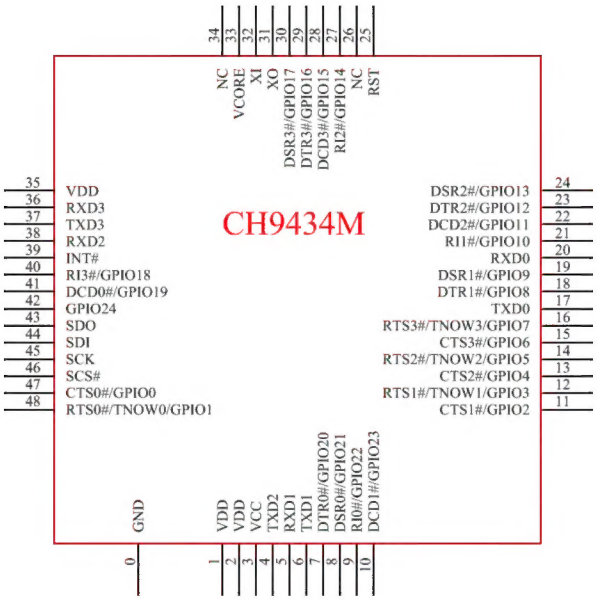
2. Features

- Operating voltage: 3.3V
- Support communication baud rate setting, with the baud rate range of 1200-4000000bps.
- UART has an independent FIFO buffer in each direction, sending 1536 bytes and receiving 2048 bytes.
- Four fully independent UARTs, compatible with 16C550 and enhanced.
- Support 5/6/7/8 data bits and 1/2 stop bits.
- UARTs support odd, even, no parity, blank 0, mark 1 and other verification methods.
- Support the commonly used MODEM communication signals RTS, DTR, DCD, RI, DSR and CTS.
- Provide half-duplex RS485 receive/transmit enable pin.
- The maximum rate of SPI is 16Mbit/s.
- Support low power sleep mode, which can be awakened via SPI interface.
- Built-in clock, which can be provided by the optional external crystal oscillator.
- Provide configurable GPIO functions.
- Provide QFN48_5X5 lead-free package, compatible with RoHS.

3. Applications

- MCU/DSP/embedded system.
- Industrial automation RS-485 communication.
- Serial server, card with multi serial ports.
- Communicate with Bluetooth, 4G, WiFi and other serial modules to realize wireless transmission.

4. Package



Package	Width of Plastic	Pitch of Pin		Instruction of Package	Ordering Information
QFN48_5X5	5*5mm	0.35mm	13.8mil	Square leadless 48-pin	CH9434M

5. Pin

Pin No.	Pin Name	Pin Type	Pin Description
0	GND	P	Power ground
1	VDD	P	The internal power supply of the chip needs to be externally connected to a decoupling capacitor if short-circuited with other VDD. The capacitance value is recommended not to be less than 0.1uF.
2	VDD	P	Internal power supply of the chip, short-circuited with other VDD.
3	VCC	P	The internal power supply of the chip needs to be externally connected to a decoupling capacitor with the capacitance of no less than 0.1uF.
4	TXD2	O	Serial data output of UART2
5	RXD1	I	Serial data input of UART1
6	TXD1	O	Serial data output of UART1
7	DTR0# /GPIO20	I/O	DTR0#: MODEM output signal of UART0; data terminal is ready. GPIO20: General purpose two-way digital I/0 pin
8	DSR0# /GPIO21	I/O	DSR0#: MODEM input signal of UART0; data device is ready. GPIO21: General purpose two-way digital I/0 pin
9	RI0# /GPIO22	I/O	RI0#: MODEM input signal of UART0; ring indicator. GPIO22: General purpose two-way digital I/0 pin
10	DCD1# /GPIO23	I/O	DCD1#: MODEM input signal of UART1; carrier detection. GPIO23: General purpose two-way digital I/0 pin
11	CTS1#	I/O	CTS1#: MODEM communication input signal of UART1; clear to send,

	/GPIO2		active at low level GPIO2: General purpose two-way digital I/0 pin
12	RTS1# /TNOW1 /GPIO3	I/O	RTS1#: MODEM communication output signal of UART1; request to send, active at low level TNOW1: RS485 receive/transmit switch control pin of UART1 GPIO3: General purpose two-way digital I/0 pin
13	CTS2# /GPIO4	I/O	CTS2#: MODEM communication input signal of UART2; clear to send, active at low level GPIO4: General purpose two-way digital I/0 pin
14	RTS2# /TNOW2 /GPIO5	I/O	RTS2#: MODEM communication output signal of UART2; request to send, active at low level TNOW2: RS485 receive/transmit switch control pin of UART2 GPIO5: General purpose two-way digital I/0 pin
15	CTS3# /GPIO6	I/O	CTS3#: MODEM communication input signal of UART3; clear to send, active at low level GPIO6: General purpose two-way digital I/0 pin
16	RTS3# /TNOW3 /GPIO7	I/O	RTS3#: MODEM communication output signal of UART3; request to send, active at low level TNOW3: RS485 receive/transmit switch control pin of UART3 GPIO7: General purpose two-way digital I/0 pin
17	TXD0	O	Serial data output of UART0
18	DTR1 /GPIO8	I/O	DTR1#: MODEM output signal of UART1; data terminal is ready. GPIO8: General purpose two-way digital I/0 pin
19	DSR1 /GPIO9	I/O	DSR1#: MODEM input signal of UART1; data device is ready. GPIO9: General purpose two-way digital I/0 pin
20	RXD0	I	Serial data input of UART0
21	RI1# /GPIO10	I/O	RI1#: MODEM input signal of UART1; ring indicator. GPIO10: General purpose two-way digital I/0 pin
22	DCD2# /GPIO11	I/O	DCD2#: MODEM input signal of UART2; carrier detection. GPIO11: General purpose two-way digital I/0 pin
23	DTR2# /GPIO12	I/O	DTR2#: MODEM output signal of UART2; data terminal is ready. GPIO12: General purpose two-way digital I/0 pin
24	DSR2# /GPIO13	I/O	DSR2#: MODEM input signal of UART2; data device is ready. GPIO13: General purpose two-way digital I/0 pin
25	RST	I	Chip reset pin, active at low level
26	NC	N	Invalid pin, suspended
27	RI2# /GPIO14	I/O	RI2#: MODEM input signal of UART2; ring indicator. GPIO14: General purpose two-way digital I/0 pin
28	DCD3# /GPIO15	I/O	DCD3#: MODEM input signal of UART3; carrier detection. GPIO15: General purpose two-way digital I/0 pin
29	DTR3# /GPIO16	I/O	DTR3#: MODEM output signal of UART3; data terminal is ready. GPIO16: General purpose two-way digital I/0 pin
30	DSR3# /GPIO17	I/O	DSR3#: MODEM input signal of UART3; data device is ready. GPIO17: General purpose two-way digital I/0 pin
31	XO	A	Inverted output terminal of high-frequency crystal oscillator

32	XI	A	Inverted input terminal of high-frequency crystal oscillator
33	VCORE	P	Internal chip power supply, which is required to be close to the external decoupling capacitor of the pin. The capacitance value is recommended not to be less than 0.1uF.
34	NC	N	Invalid pin, suspended
35	VDD	P	The internal power supply of the chip needs to be externally connected to a decoupling capacitor if short-circuited with other VDD. The capacitance value is recommended not to be less than 0.1uF.
36	RXD3	I	Serial data input of UART3
37	TXD3	O	Serial data output of UART3
38	RXD2	I	Serial data input of UART2
39	INT#	O	Interrupt output pin, active at low level
40	RI3# /GPIO18	I/O	RI3#: MODEM input signal of UART3; ring indicator. GPIO18: General purpose two-way digital I/0 pin
41	DCD0# /GPIO19	I/O	DCD0#: MODEM input signal of UART0; carrier detection. GPIO19: General purpose two-way digital I/0 pin
42	GPIO24	I/O	GPIO24: General purpose two-way digital I/0 pin
43	SDO	O	SPI serial data output
44	SDI	I	SPI serial data input
45	SCK	I	SPI serial clock input
46	SCS#	I	SPI chip selection input, active at low level
47	CTS0# /GPIO0	I/O	CTS0#: MODEM communication input signal of UART0; clear to send, active at low level GPIO0: General purpose two-way digital I/0 pin
48	RTS0# /TNOW0 /GPIO1	I/O	RTS0#: MODEM communication output signal of UART0; request to send, active at low level TNOW0: RS485 receive/transmit switch control pin of UART0 GPIO1: General purpose two-way digital I/0 pin

Note: P: power pin; I: input pin; O: output pin; N: empty pin

The multiplexing function takes precedence.

6. Clock Configuration

The CH9434 chip can choose to use the chip's internal clock source or an external crystal to cooperate with the chip's internal clock oscillator to provide a 32MHz input clock. UART reference clock can be directly generated by the input clock or by turning on the clock frequency multiplication and frequency demultiplication. It is provided to UART0- UART3. The frequency multiplication factor is fixed at 15, and the frequency demultiplication factor is configured through the R8_CLK_CTRL_CFG register.

When the clock multiplication is enabled, UART reference clock = 32MHz * multiplication factor/demultiplication factor. It is recommended that the frequency demultiplication factor is configured as 13 when using the regular baud rate. The chip clock mode can be configured when CH9434 is initialized, and other operations need to be delayed for a period of time after configuration.

7. Register

7.1 Serial Port Register

The CH9434 chip provides four separate UART modules, each configured using a separate 8-byte register. The addresses are: 00H-07H for UART0, 10H-17H for UART1, 20H-27H for UART2 and 30H-37H for UART3. The serial register is compatible with the industry standard 16C550 or 16C750 and has been enhanced. In the table, DLAB is bit 7 of the register LCR, X means that the value of DLAB is not concerned, RO means the register is read-only, WO means the register is write-only, and R/W means the register is readable and writable.

Add:	DLAB	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	R0	RBR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	W0	THR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	R/W	IER	RESET	LOWPOWER	0	0	IEMODEM	IELINES	IETHRE	IERECV
2	X	R0	IIR	FIFOENS	FIFOENS	0	0	IID3	IID2	IID1	NOINT
2	X	W0	FCR	RECVTG1	RECVTG0	0	0	0	TFIFORST	RFIFORST	FIFOEN
3	X	R/W	LCR	DLAB	BREAKEN	PARMODE1	PARMODE0	PAREN	STOPBIT	WORDSZ1	WORDSZ0
4	X	R/W	MCR	0	0	AFE	LOOP	OUT2	OUT1	RTS	DTR
5	X	R0	LSR	RFIFOERR	TEMT	THRE	BREAKINT	FRAMEERR	PARERR	OVERR	DATARDY
6	X	R0	MSR	DCD	RI	DSR	CTS	△ DCD	△ RI	△ DSR	△ CTS
7	X	R/W	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	R/W	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	R/W	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

The following table shows the default of the serial port register after power-on reset or serial port soft reset.

Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IER	0	0	0	0	0	0	0	0
IIR	0	0	0	0	0	0	0	1
FCR	0	0	0	0	0	0	0	0
LCR	0	0	0	0	0	0	0	0
MCR	0	0	0	0	0	0	0	0
LSR	0	1	1	0	0	0	0	0
MSR	DCD	RI	DSR	CTS	0	0	0	0
SCR	Keep	Keep	Keep	Keep	Keep	Keep	Keep	Keep
FIFO	Reset, including FIFO transmitting and FIFO receiving							
TSR	Reset; TSR is the UART transmitter shift register							
RSR	Reset; RSR is the UART receiving shift register							
Other	is not defined							

RBR: Receiving buffer register. If the DATARDY bit of LSR is 1, the received data can be read from this register. If FIFOEN is 1, the data received from UART shift register RSR will be firstly stored in the receiver FIFO, and then read out through the register.

THR: Transmitter holding register, including transmitting FIFO, for writing the data to be transmitted. If FIFOEN is 1, the written data will be firstly stored in the transmit FIFO, and then output one by one through the transmitter shift register TSR.

IER: Interrupt enabling register, including enhanced function control bit and serial port interrupt enabling.

RESET: When this bit is set to 1, soft reset the serial port, and this bit can be cleared automatically

without software clearing.

LOWPOWER: When this bit is 1, the internal reference clock of UART will be turned off, so that UART will enter a low power consumption status.

IEMODEM: When this bit is 1, it will allow modem input status change interrupt.

IELINES: When this bit is 1, it will allow receiver line status interrupt.

IETHRE: When this bit is 1, it will allow transmitter holding register null interrupt.

IERECV: When this bit is 1, it will allow received data interrupt.

IIR: Interrupt recognition register, for analyzing the interrupt source and processing.

FIFOENS: This bit is the FIFO enabled status, and 1 means that the FIFO has been enabled.

IIR register bit				Priority	Interrupt Type	Interrupt sources	Method for clearing interrupt
II D3	II D2	II D1	NOINT				
0	0	0	1	None	No interrupt generated	No interrupt	
0	1	1	0	1	Receiving line status	OVERR, PARERR, FRAMEERR, BREAKINT	Reading LSR
0	1	0	0	2	Receiving data available	The number of bytes received reaches the trigger point of FIFO	Reading RBR
1	1	0	0	2	Data receiving timeout	No next data is received when the time of four data is exceeded	Reading RBR
0	0	1	0	3	THR register null	Transmitter holding register null, IETHRE changes from 0 to 1 to re-enable the interrupt	Reading IIR Or writing THR
0	0	0	0	4	MODEM input change	△ CTS, △ DSR, △ RI, △ DCD	Reading MSR

FCR: First-in-first-out buffer area FIFO control register, used to enable and reset FIFO.

RECVTG1 and RECVTG0: Set the trigger point for receiver FIFO interrupt and hardware flow control. 00 corresponds to 256 bytes, that is, interrupt available for receiving data is generated when 256 bytes are received, and RTS pin is automatically invalid when hardware flow control is enabled. 01 corresponds to 512 bytes, 10 corresponds to 1024 bytes, and 11 corresponds to 1280 bytes.

TFIFORST: When this bit is set to 1, the data in the FIFO transmitting (not including TSR) will be cleared. This bit can be cleared automatically without software clearing.

RFIFORST: When this bit is set to 1, the data in the FIFO transmitting (not including RSR) will be cleared. This bit can be cleared automatically without software clearing.

FIFOEN: When this bit is 1, FIFO will be enabled. When this bit is cleared, FIFO will be disabled. After FIFO is disabled, it will be 16C450 compatible mode, which is equivalent to only one byte in FIFO.

LCR: Line control register, used to control the format of serial communication.

DLAB: This bit is the access enabling of the divisor latch. When it is 1, DLL and DLM can be accessed; when it is 0, RBR/THR/IER can be accessed.

BREAKEN: When this bit is 1, it is mandatory to generate a BREAK line interval.

PARMODE1 and PARMODE0: When PAREN is 1, set the format of the parity bit: 00 means odd parity, 01 means even parity, 10 means mark bit (MARK, set to 1), 11 means blank bit (SPACE,

cleared).

PAREN: When this bit is 1, it is allowed to generate parity bit during transmission and check parity bit when receiving. If it is 0, there is no parity bit.

STOPBIT: When this bit is 1, there will be two stop bits. When it is 0, there will be one stop bit.

WORDSZ1 and WORDSZ0: Set the word length; 00 means 5 data bits, 01 means 6 data bits, 10 means 7 data bits, and 11 means 8 data bits.

MCR: Modem control register, used to control MODEM output.

AFE: When this bit is 1, the hardware automatic flow control of CTS and RTS is allowed. If AFE is 1, then the serial port will continuously send the next data only when it detects that the CTS pin input is valid (active at low level). Otherwise, the serial port transmission will be suspended. If AFE is 1 and RTS is 1, the serial port will automatically validate the RTS pin (active at low level) when receiver FIFO is null. The serial port will automatically invalidate the RTS pin when the number of received bytes reaches the trigger point of FIFO and will re-validate the RTS pin when the receiver FIFO is null. You can connect your own CTS pin to the other party's RTS pin through the hardware automatic band rate control, and can connect your own RTS pin to the other party's CTS pin.

LOOP: When this bit is 1, the test mode of the internal loop will be enabled. In the test mode of the internal loop, all external output pins of the serial port are at the invalid status, TXD internally returns to RXD (i.e., the output of TSR internally returns to the input of RSR), RTS internally returns to CTS, DTR internally returns to DSR, OUT1 internally returns to RI and OUT2 internally returns to DCD.

OUT2: If this bit is 1, the interrupt request output of the serial port is allowed. Otherwise, the serial port will not generate the actual interrupt request.

OUT1: This bit is a user-definable MODEM control bit, and no actual output pin is connected.

RTS: If this bit is 1, the RTS pin output will be valid (active at low level). Otherwise, the RTS pin output will be invalid.

DTR: If this bit is 1, the DTR pin output will be valid (active at low level). Otherwise, the DTR pin output will be invalid.

LSR: Line status register, used for querying and analyzing the status of the serial port.

RFIFOERR: When this bit is 1, it means that there is at least one PARERR, FRAMEERR or BREAKINT error in the receiver FIFO.

TEMT: When this bit is 1, it means that the transmitter holding register(THR) and the transmitter shift register (TSR) are both null.

THRE: When this bit is 1, it means that the transmitter holding register(THR) is null.

BREAKINT: When this bit is 1, it means that the BREAK line interval is detected.

FRAMEERR: When this bit is 1, it means the frame error of the data being read from the receiver FIFO due to lack of a valid stop bit.

PARERR: When this bit is 1, it means the parity error of the data being read from the receiver FIFO.

OVERR: When this bit is 1, it means that the receiver FIFO buffer area has overflowed.

DATARDY: When this bit is 1, it means that there is received data in the receiver FIFO. After reading all the data in the FIFO, this bit will be automatically cleared.

MSR: Modem status register, used to query the Modem status.

DCD: This bit is the reverse bit of the DCD pin. When it is 1, it means that the DCD pin is valid (active at low level).

RI: This bit is the reverse bit of the RI pin. When it is 1, it means that the RI pin is valid (active at low level).

DSR: This bit is the reverse bit of the DSR pin. When it is 1, it means that the DSR pin is valid

(active at low level).

CTS: This bit is the reverse bit of the CTS pin. When it is1, it means that the CTS pin is valid (active at low level).

△ DCD: When this bit is 1, it means that the DCD pin input status has changed.

△ RI: When this bit is 1, it means that the input status of the RI pin has changed.

△ DSR: When this bit is 1, it means that the input status of the DSR pin has changed.

△ CTS: When this bit is 1, it means that the input status of the CTS pin has changed.

SCR: The user can define the register.

DLL and DLM: Baud rate divisor latch. DLL is the low byte and DLM is the high byte. The 16-bit divisor formed by the two is used for UART baud rate generator composed of a 16-bit counter. The divisor = the reference clock of the UART / 8 / the required communication baud rate.

7.2 Interface Register

Address	Name	Function	(Bit)	Access	Bit Definition	Default Value
41H	R8_TNOW_CTRL_CFG	TNOW function setting	[7:4]	R/W	TNOW pin level reverse phase	0000b
			[3:0]	R/W	TNOW pin function control	0000b
42H	R8_FIFO_CTRL	FIFO counter setting	[7:5]	RO	Reserved	000b
			4	R/W	Receive/transmit buffer control 0: Receiver FIFO; 1: Transmitter FIFO.	0
			[3:0]	R/W	UART number	0000b
43H	R8_FIFO_CNT_L	FIFO counter	[7:0]	RO	Low 8 bits of FIFO counter	XXh
44H	R8_FIFO_CNT_H	FIFO counter	[7:0]	RO	High 8 bits of FIFO counter	XXh

R8_TNOW_CTRL_CFG: Set to enable/disable the TNOW function and polarity. When the polarity defaults to sending data, the corresponding TNOW pin is pulled up, and TNOW is pulled down after sending.

R8_FIFO_CTRL: FIFO counter setting. After setting the FIFO direction and UART number, read the values of R8_FIFO_CNT_L and R8_FIFO_CNT_H and then correspond to the read FIFO counter.

Among them: The read UART transmitter FIFO counter value is the current remaining FIFO quantity, and the master control can fill in the maximum number of transmitter data according to this value; the read receiver FIFO counter value is the quantity of current received data, and the master control can use this value to read all serial data.

7.3 Clock Power Register

Address	Name	Function	(Bit)	Access	Bit Definition	Default Value
48H	R8_CLK_CTRL_CFG	Chip clock settings	[7:6]	R/W	HCLK system clock source mode selection: 00: Internal 32M 01: External crystal oscillator	00b

					10: Use internal 32M and enable frequency multiplication 11: Use external crystal oscillator and enable frequency multiplication	
			5	R/W	External oscillator power switch	0
			[4:0]	R/W	Frequency division coefficient	15
4AH	R8_SLEEP_MOD_CFG	Sleep function settings	[7:3]	RO	Reserved	00000b
			[2:0]	R/W	Chip low power settings 0: Do not enter the low power state; 1: SLEEP state; 2-7: Reserved.	000b

R8_CLK_CTRL_CFG: Chip clock settings, use the internal clock 32MHz of the chip by default. The frequency demultiplication coefficient is enabled after the frequency multiplication function is enabled.

For conditions where the application requirements are not very high, the internal clock can be used. In general, the error is within 3%, and the error does not exceed 1% in the range of -5°C to 70°C. For more demanding applications, it is recommended to externally connect a crystal with the internal clock oscillator of the chip to provide the clock.

7.4 GPIO Register

Address	Name	Function	(Bit)	Access	Bit Definition	Default Value
50H	R8_GPIO_FUNC_EN_0	GPIO7-0 Enable	[7:0]	R/W	[7:0] Corresponding GPIO7-0 enable control 0: Disable GPIO function 1: Enable GPIO function	00h
51H	R8_GPIO_FUNC_EN_1	GPIO15-8 Enable	[7:0]	R/W	[7:0] Corresponding GPIO15-8 enable control, values are defined as above	00h
52H	R8_GPIO_FUNC_EN_2	GPIO23-16 Enable	[7:0]	R/W	[7:0] Corresponding GPIO23-16 enable control, values are defined as above	00h
53H	R8_GPIO_FUNC_EN_3	Reserved	[7:1]	RO	Reserved	00000000b
		GPIO24 Enable	0	R/W	Corresponding GPIO24 enable control, values are defined as above	0b
54H	R8_GPIO_DIR_MOD_0	GPIO7-0 Direction settings	[7:0]	R/W	[7:0] Corresponding GPIO7-0 direction settings 0: GPIO set as input 1: GPIO set as output	00h

55H	R8_GPIO_DIR_MOD_1	GPIO15-8 Direction settings	[7:0]	R/W	[7:0] Corresponding GPIO15-8 direction settings, values are defined as above	00h
56H	R8_GPIO_DIR_MOD_2	GPIO23-16 Direction settings	[7:0]	R/W	[7:0] Corresponding GPIO23-16 direction settings, values are defined as above	00h
57H	R8_GPIO_DIR_MOD_3	Reserved	[7:1]	RO	Reserved	00000000b
		GPIO24 Direction settings	0	R/W	Corresponding GPIO24 direction settings, values are defined as above	0b
58H	R8_GPIO_PU_MOD_0	GPIO7-0 Pull-up resistor settings	[7:0]	R/W	[7:0] Corresponding GPIO7-0 pull-up resistor settings 0: Disable GPIO pull-up resistor 1: Enable GPIO pull-up resistor	00h
59H	R8_GPIO_PU_MOD_1	GPIO15-8 Pull-up resistor settings	[7:0]	R/W	[7:0] Corresponding GPIO15-8 pull-up resistor settings, values are defined as above	00h
5AH	R8_GPIO_PU_MOD_2	GPIO23-16 Pull-up resistor settings	[7:0]	R/W	[7:0] Corresponding GPIO23-16 pull-up resistor settings, values are defined as above	00h
5BH	R8_GPIO_PU_MOD_3	Reserved	[7:1]	RO	Reserved	00000000b
		GPIO24 Pull-up resistor settings	0	R/W	Corresponding GPIO24 pull-up resistor settings, values are defined as above	0b
5CH	R8_GPIO_PD_MOD_0	GPIO7-0 Pull-down resistor settings	[7:0]	R/W	[7:0] Corresponding GPIO7-0 pull-down resistor settings 0: Disable GPIO pull-down resistor 1: Enable GPIO pull-down resistor	00h
5DH	R8_GPIO_PD_MOD_1	GPIO15-8 Pull-down resistor settings	[7:0]	R/W	[7:0] Corresponding GPIO15-8 pull-down resistor settings, values are defined as above	00h
5EH	R8_GPIO_PD_MOD_2	GPIO23-16 Pull-down resistor settings	[7:0]	R/W	[7:0] Corresponding GPIO23-16 pull-down resistor settings, values are defined as above	00h
5FH	R8_GPIO_PD_MOD_3	Reserved	[7:1]	RO	Reserved	00000000b
		GPIO24	0	R/W	Corresponding GPIO24	0b

		Pull-down resistor settings			pull-down resistor settings, values are defined as above	
60H	R8_GPIO_PIN_VAL_0	GPIO7-0 Input/output level	[7:0]	R/W	[7:0] Corresponding GPIO7-0 pin level When write register GPIO is output: 1: Output high level 0: Input low level When read register GPIO is input: Pin level state	00h
61H	R8_GPIO_PIN_VAL_1	GPIO15-8 Input/output level	[7:0]	R/W	[7:0] Corresponding GPIO15-8 pin level, values are defined as above	00h
62H	R8_GPIO_PIN_VAL_2	GPIO23-16 Input/output level	[7:0]	R/W	[7:0] Corresponding GPIO23-16 pin level, values are defined as above	00h
63H	R8_GPIO_PIN_VAL_3	Reserved	[7:1]	RO	Reserved	00000000b
		GPIO24 Input/output level	0	R/W	Corresponding GPIO24 pin level, values are defined as above	0b

GPIO setting method:

(1) Enable the corresponding GPIO enable bit;

(2) Set pull-up/down resistor configuration and direction;

(3) Set or read the "input/output level" register. When setting the register, the corresponding bit is processed when the GPIO direction is output, and the corresponding level value is output. The input pin does not relate to the corresponding bit; when reading the register, the corresponding bit is processed when the GPIO direction is input, and the output pin does not relate to the corresponding bit.

For GPIOs not included in the chip, the related register definition is invalid.

8. Functional Specification

8.1 Interrupt and Query

The INT# pin of CH9434 chip is the interrupt request output pin. The default pin is in the pull-up output mode after the chip is powered on, which is active at low level. Since the four UARTs share an interrupt pin output, when there is an interrupt valid signal, the master MCU needs to query the interrupt status of all UARTs to analyze which UART has an interrupt request.

If UART has multiple interrupt request outputs, when the master MCU reads a valid interrupt status, CH9434 will temporarily raise the interrupt pin and then lower it. The master MCU can query and judge. As long as the interrupt pin is at low level, UART interrupt status can be directly inquired.

8.2 Serial Port Operation

The operation of the serial port provides IIR and LSR registers to query the status of UART. CH9434 also expands a FIFO register to directly obtain the current transceiving data volume of UART of the chip.

When UART interrupts inquire that there is received data, it can first read the receiver FIFO length of the current UART, and then directly operate the RBR register to read all the data. The master MCU can also simplify the processing and directly query the data volume currently received by FIFO regularly, and then operate the RBR register to read the data according to the quantity of the receiver FIFO.

To send data, the master MCU can query the empty status of the sending buffer of the IIR and LSR registers, and then operate the THR register to send data through UART. The master MCU can also simplify the processing and transmit data by querying the FIFO size. The value of the transmitter FIFO data length queried is the remaining FIFO size, and the master MCU can use this size to fill the transmission data into the THR register for data transmission.

The serial flow control function is enabled by setting the AFE bit to 1, and CH9434 will automatically perform hardware flow control. The chip will automatically operate the flow control pin according to the FIFO size. After enabling automatic flow control, the chip UART will continuously send data when CTS is valid; and when the CTS pin is invalid, UART will stop sending after sending up to 8 bytes of data. RTS is automatically invalidated when the FIFO is triggered to reach the set number of flow control bytes.

8.3 RS485 Switch Pin TNOW

The CH9434 UART provides RS485 switch pin TNOW. The pin function is multiplexed with other functions. When the TNOW function is enabled, the original MODEM signal function will be automatically invalidated. TNOW also supports polarity adjustment to adapt to different polarity usage scenarios.

8.4 GPIO Function

CH9434 supports multiplexing function pins as GPIO functions, and supports up to 25 channels. Each IO can independently set the direction, pull-up resistor and pull-down resistor configuration. After the GPIO function is enabled, other multiplexing functions of the IO will be automatically invalidated.

8.5 Low-power Mode

CH9434 supports low power consumption mode setting. After setting the SLEEP mode, the chip suspends operation, the current consumption can be reduced to less than 1.5mA, and the SPI can be directly operated to wake up the chip.

8.6 SPI Serial Interface

The SPI synchronous serial signal lines include: SPI chip selection input pin SCS#, serial clock input pin SCK, serial data input pin SDI and serial data output pin SDO. SPI data bit sequence: MSB first. The format of sending data is that the first byte is the operation address, the second byte is the data written or read, and the highest bit of the operation address is the operation bit. An operation bit of 1 is written data, and a bit of 0 is read data. When writing data, a 1uS delay is required between the two bytes of the address and the data. After the data is sent, a delay of 3uS is required before the next operation can be performed. When reading data, the address and data need to be delayed by 3uS, that is, after sending the address, a delay of 3uS is required to read the data.

9. Parameters

9.1 Absolute Maximum Value

Critical value or exceeding the absolute maximum value may cause the chip to work abnormally or even be

damaged.

Name	Parameter description	Min.	Max.	Unit
TA	Ambient temperature during operation	-40	85	℃
TS	Ambient temperature during storage	-40	105	℃
VCC	Supply voltage (VCC connects to power, GND to ground)	-0.4	3.9	V
VIO	Voltage on the input or output pins	-0.4	VCC+0.4	V

9.2. Electrical Parameters

Test Conditions: TA=25℃, VCC=3.3V

Name	Parameter description	Min.	Typ.	Max.	Unit
VCC	System supply voltage	2.4	3.3	3.6	V
ICC	Total supply current during operation	2.3	3.8		mA
VIL	Low level input voltage	0		0.9	V
VIH	High level input voltage	2.0		VCC	V
VOL	Low level output voltage	0	0.3	0.4	V
VOH	High level output voltage	VCC-0.4	VCC-0.3	VCC	V
IDN	Input current at the input terminal with the built-in pull-down resistor	-90	-60	25	uA
IUP	Input current at the input terminal with the built-in pull-up resistor	25	60	90	uA